# Efficient Topology of Voltage Source Inverter with Reduced number of Transistors

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**Abstract:**

An advanced topology of Voltage Source Inverter has been introduced in this paper. The usage of low-cost switching devices such as Thyristor give some edge to improved topology over conventional topology. The traditional topology requires six transistor, whereas on the contrary it possess only three high performance transistors. The conventional topology could prove to be expensive for high power applications where costly switching devices such as silicon carbide and gallium nitride are required thus, the new evolving topology could be more feasible for it. Simulation and experimental results have been provided for further verification.

*Keywords: Efficient Topology, Inverter, VSI, Transistor, Thyristor*

## 1. Introduction

Semiconductor devices like bipolar junction transistors, MOSFETs, Thyristors, Triac and Diac, etc. make our lives easier. They act as an intermediate between various forms of energies and convert one form of power into another form. These all small devices combine together and make a huge sea of revolutionary machines. Initially electromechanical converters derived one form of energy into another form. Inverter is basically a converter which convert DC power into AC power. The word "inverter" is derived from a class of power electronics circuits which could be able to operate from a DC voltage source or DC current source and convert it into AC voltage or AC current [1-3]. Although it is not unusual that the input DC supply could get from the AC source the primary source is AC, it is converter from AC

to DC converter into DC form and then converted back to AC using an inverter. Since the resultant output might be different in frequency and magnitude from the initial AC supply [4]. Now a days, we use a common topology which we call it conventional topology here and it is shown in Figure 1. It is widely used in many applications like Un-interruptible Power Supply (UPS), Industrial motor drives, HVDC etc. This paper focused on the proposal of three-phase voltage source inverter (VSI) which has similar features compared to the conventional topology of six switches (transistor) in terms of voltage-current waveforms. In this paper, a topology is introduced which has a major reduction of transistors and instead of these inexpensive thyristors are used shown in Figure 2.

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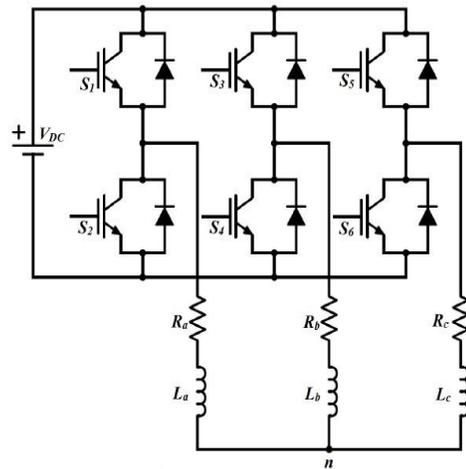
**Fig 1**: Schematic model of proposed topology
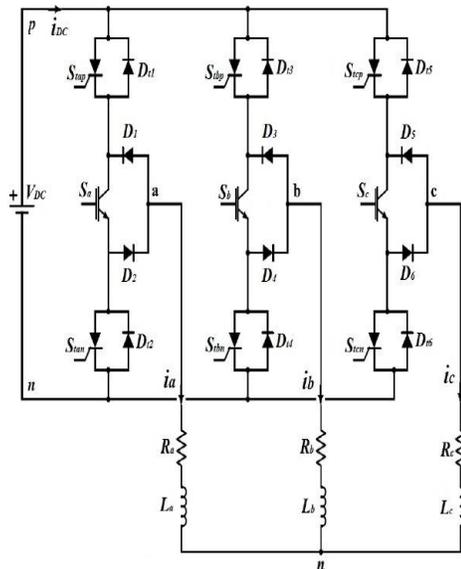


**Fig 2:** Schematic model of Conventional topology

This paper discusses the proposed topology, its basic operation and switching technique. Software implementation of the topology is implemented using MATLAB/SIMULINK and also its Experimental results are provided to analyse and verify its feasibility and performance.

## 2. Proposed Topology

Inverters are power electronics converters which convert Direct Current (DC) into Alternating Current (AC) utilized extensively in many applications such as induction heating, variable speed AC motor derives Distributed Generation (DG) and Uninterrupted Power Supplies (UPS).

Semiconductor electronic switches are one of the major components of the converter which essentially determine the complexity, cost and efficiency of the system. Mostly, silicon-based power electronic switches are widely used in the market [5].

Here the proposed novel topology of three leg Voltage Source Inverter (VSI) (shown in Figure 2) which possesses three semiconductor transistors unlike the conventional topology which contain six semiconductor transistors. This makes this topology cost effective [6]. Thyristors are also present per phase to provide natural commutation Therefore, there is no need of external commutation circuitry. This topology is more efficient and cost effective than conventional topologies of Voltage Source Inverters (VSI).

## 3. Commutation Scheme for Novel Topology

It includes switching elements like transistors and thyristors which require a proper switching technique to drive the required results. Commutation speed of such devices could be controllable. Direction of positive and negative current flow will be discussed in this section. Only one phase of this topology will be elaborated here in order to understand its functionality properly [7].

### A. Basic commutation operation

a) Positive Current Control Scheme

   i   For positive cycle of current flow, thyristor Stap will remain on while keeping the complimentary thyristor Stan off. As shown in the Figure 3(a).

   ii   With the help of an appropriate PWM technique transistor Sa will continuously turn on and off.

   iii   Positive current direction remains through Stap, Sa, D2, and Dt2, in the whole positive current cycle.

   iv   At zero crossing of a single period, the gate signal from transistor Sa should be removed to turn off the thyristor Stap
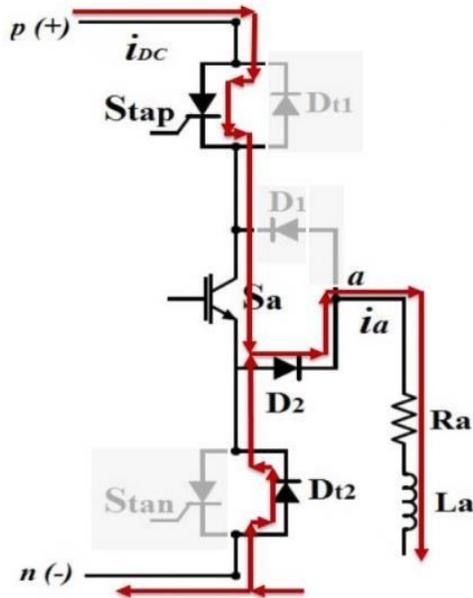
**Fig 3(a):** Current Control Scheme for Single Phase
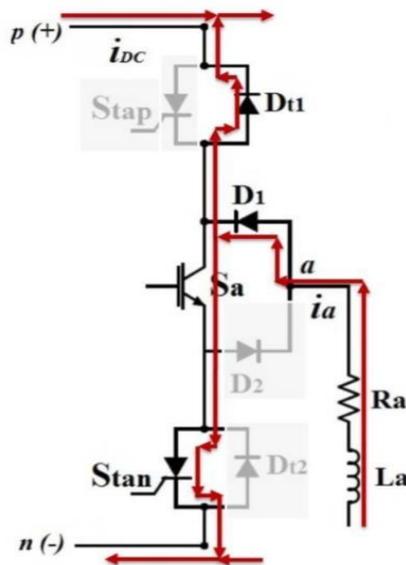


**Fig 3(b):** Current Control Scheme for Single Phase

b) Negative Current Control Scheme

  i   For negative cycle of current flow, thyristor Stap will remain on while keeping the complimentary thyristor Stap off. As shown in the Fig 3(b).

  ii   With the help of an appropriate PWM technique transistor Sa will continuously turn on and off.

  iii   Current direction Negative remains through Stan, Sa, D1, and Dt1, in the whole positive current cycle.

  iv   For remaining stages, the same process will be repeated with respect to their phase order.

## 4. Switching States of Novel Topology

This Novel Topology of VSI which contain three stages (three legs) has total eight active and zero voltage commutation stages like conventional topology. In Figure 4(a) to Figure 4(f), only the active elements and the path of current flow are elaborated here. These are the six active commutation stages. At each stage there is only single thyristor and a transistor will be turned on for conduction of a phase. On the other side, the opposite thyristor of the same stage cannot conduct.

In Figure 4(a) the thyristor of third leg is conducted while its complementary thyristor remains off. When thyristor of second stage in Figure 4(b) is on, at that instance the other thyristors for positive current should be off. As shown in the Figure 4(a) only one thyristor Stcp is in conduction mode, while Stap and Stbp is turned off. The complimentary thyristors are switched on and fired off in accordance with the thyristor of same leg. As per the rule, when Stcn is off Stan and Stbn should be fired on. However, the three transistors Sa, Sb, Sc will be turned off when current reaches zero with respect to their phase. The path through thyristor Stcp, Stan, and Stbn; transistor Sa, Sb, and Sc; also, diode D1, D3, D6, Dt1, Dt3, and Dt6 followed by the current at this stage. The next commutation scheme and current flowing paths are examined in Figure 4(b) in which the active or conducted devices are shown. In addition, the pictorial description is present for the rest stages from Figure 4(c) to Figure 4(f).

(a)              (b)



(c)              (d)



(e)              (f)
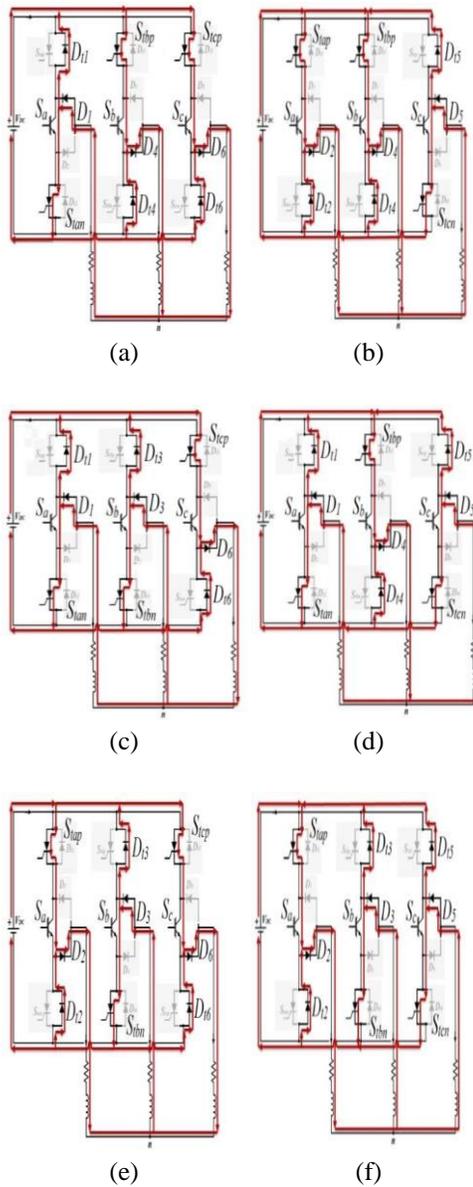
**Fig 4:** Switching States of Novel Topology

The firing sequence (switching scheme) for all thyristors and transistors are elaborated clearly in Figure 5, where the dead period between the switching of thyristors present at the same leg (Stap and Stan, Stbp and Stbn, Stcp and Stcn) is specified by the red bold mark. The transistor present in each stage is continuously commutated on and off by an appropriate PWM techniques. When this switching pulse is removed from transistors, the dead period will be generated between the commutation sequences of thyristors. It behaves in a way that when triggering signal is removed from

the transistor, the circuit acts as an open path At that time,current could not flow through the circuit. According to the commutation sequence the elimination of gate pulse from transistor switched off the thyristor and provided them an appropriate recovery time for the next stage. Below the conduction periods of semiconductor devices are illustrated in an adequate way [8].
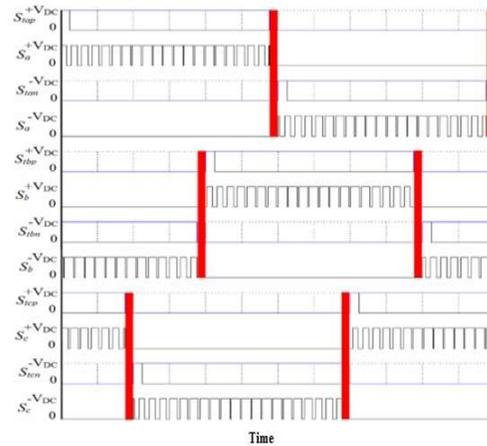


**Fig 5.** Conduction sequences of devices

According to the way of commutation illustrated in Fig 4(a) to Fig 4(f), it can be analysed that the switching sequences are:

$$Stap.Sa + Stan.Sa = 1 \quad (1)$$

$$Stbp.Sb + Stbn.Sb = 1 \quad (2)$$

$$Stcp.Sc + Stcn.Sc = 1 \quad (3)$$

The table I, elaborates the eight switching states of inverter. Non-zero out AC line voltage generated by seven stages and the rest two stages: stage 1 and stage 8 generate zero AC line voltage. The resultant line to line AC output voltage have discrete values of Vdc, 0, and −Vdc. Output line voltages are shown with respect to the conduction of their devices.

TABLE I.  Switching states of devices

| Switching States | Devices | | | Output Line | Voltages | |
|---|---|---|---|---|---|---|
| | Stap.Sa | Stb.Sb | Stcp.Sc | Vab | Vbc | Vca |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | -Vdc | Vdc |
| 3 | 0 | 1 | 0 | -Vdc | Vdc | 0 |
| 4 | 0 | 1 | 1 | -Vdc | 0 | -Vdc |
| 5 | 1 | 0 | 0 | Vdc | 0 | -Vdc |
| 6 | 1 | 0 | 1 | Vdc | -Vdc | 0 |
| 7 | 1 | 1 | 0 | 0 | Vdc | Vdc |
| 8 | 1 | 1 | 1 | 0 | 0 | 0 |

## 5.  Switching Control Scheme

It is defined before that the transistors present at the middle of each leg is commutated on and off with any specific switching scheme. Any commutation technique/triggering scheme could be utilized to provide gate pulses to the transistors. However, in this project a uniquely designed PWM scheme was generated through Sine-Triangle PWM scheme. In this method a primary Sinusoidal waveform is compared with a triangular waveform.

The same gate pulse is applied to the transistor during positive and negative cycle of waveform in order to provide commutation from positive to negative current of thyristor at each phase. For easily understanding the analytical behaviour, it is assumed that the delay between each phase of thyristor is eliminated. During the shifting from positive to negative cycle of current, the gate pulse provided to the transistor also have no dead time. At the end, combination of all these elements will result an appropriate control scheme. The control scheme is generated by the comparison of triangular carrier wave with sinusoidal waveform which is $120^0$ shifted from each other for each phase.

### a)  Stage 1 Control Scheme

Figure 6(a) shows the comparison of sinusoidal and triangular wave which results the generation of triggering pulse for middle transistor Sa illustrated in Figure 6(c) and Figure 6(e). In addition, step pulse for firing thyristor Stap and Stan is elaborated in Figure. 6(b) and Figure 6(d) respectively.
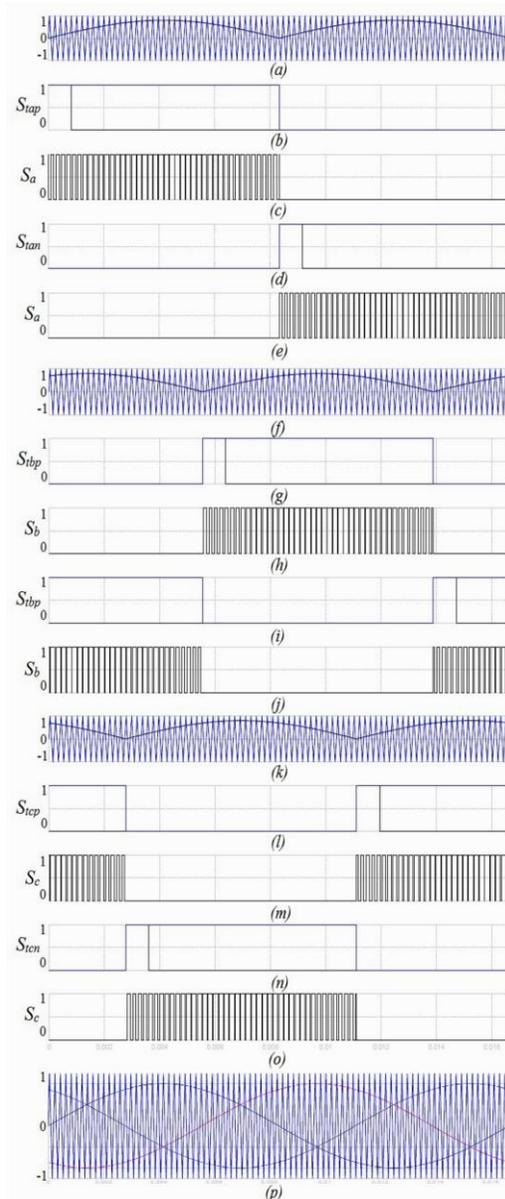


**Fig 6:** Switching Control Scheme for stage 1, 2 and 3

## b) Stage 2 Control Scheme

Switching sequence for stage 2 could also analyze in the Figure 6. In which Figure 6(g) and Figure 6(i) are exciting pulse for thyristor Stbp and Stbn respectively. The output switching gate pulse derived from the comparison of Triangular and Sinusoidal waveform as shown in Figure 6 (f), could be examined in Figure 6 (h) and Figure 6 (j). Here the sine wave has a phase difference of 1200 from previous stage [9-10].

## c) Stage 3 Control Scheme

As mentioned earlier, Figure 6 (k) reflects the comparison of sine triangle waveform where sine wave possesses 2400 phase shift than the sine wave used in first stage. Figure 6(l) and Figure 6(n) illustrate the thyristor triggering pulses (Stcp and Stcn). Figure 6(m) and Figure 6(o) illustrate the switching pulse of transistor.

## Output Current Equations

The output currents could be assumed that are:

$$i_a = I_o \, Cos(\, \omega_o t + \varphi_o \,) \qquad (4)$$

$$i_b = I_o \, Cos(\, \omega_o t + \varphi_o - \tfrac{2\pi}{3} \,) \quad (5)$$

$$i_c = I_o \, Cos(\, \omega_o t + \varphi_o + \tfrac{2\pi}{3} \,) \quad (6)$$

## Output Voltage Equations

The inverter output equation is considered as:

$$\begin{pmatrix} Va \\ Vb \\ Vc \end{pmatrix} = \begin{pmatrix} Stap & Stan \\ Stbp & Stbn \\ Stcp & Stcn \end{pmatrix} * \begin{pmatrix} Vp \\ Vn \end{pmatrix} + \begin{pmatrix} Sap & San \\ Sbp & Sbn \\ Scp & Scn \end{pmatrix} * \begin{pmatrix} Vp \\ Vn \end{pmatrix} \quad (7)$$

The value of S would be 1 when the respective switch is on. When the switch is turned off the value of S would be 0.

## Equations for Phase Voltage

By using Sine-Triangle PWM scheme equations for the phase voltages could be written as:

$$Vax = V_o \, Cos \, \omega_o t = M V_{DC} \, Cos \, \omega_o t \quad (8)$$

$$Vbx = V_o \, Cos(\, \omega_o t - \tfrac{2\pi}{3} \,) = M V_{DC} \, Cos(\, \omega_o t - \tfrac{2\pi}{3} \,) \qquad (9)$$

$$Vcx = V_o \, Cos(\, \omega_o t + \tfrac{2\pi}{3} \,) = M V_{DC} \, Cos(\, \omega_o t + \tfrac{2\pi}{3} \,) \qquad (10)$$

Line-line three phase output voltages can be defined as:

$$V_{ab} = Vax - Vbx = M \sqrt{3} \, V_{DC} \, Cos (\, \omega_o t + \tfrac{\pi}{6} \,) \qquad (11)$$

$$V_{bc} = Vbx - Vcx = M \sqrt{3} \, V_{DC} \, Cos(\, \omega_o t - \tfrac{\pi}{2} \,) \qquad (12)$$

$$V_{ca} = Vcx - Vax = M \sqrt{3} \, V_{DC} \, Cos(\, \omega_o t + \tfrac{5\pi}{6} \,) \qquad (13)$$

In the above equations

$M$ = Modulation index = $V_o / V_{DC}$

$V_o$ = peak amplitude of output voltage [13].

Hence, through these switching patterns it is understandable the working principle of three leg three phase voltage source inverter.

## 6. Simulation Results

The Novel topology is implemented using MATLAB/SIMULINK shown in Figure. 7. Simulation has been performed to observe the output current, Line voltages and Total Harmonic Distortion (THD). All the switches and the components as ideal. Simulation parameters taken for analysis are as follows:

**Input**

DC Voltage: 200 V (Peak to Peak)

**Output**

Inductance: 25 mH;

Output Resistance: 10 Ω;

Carrier Frequency: 2400 Hz:

Modulation Index: 0.8;
Output Frequency: 50 Hz
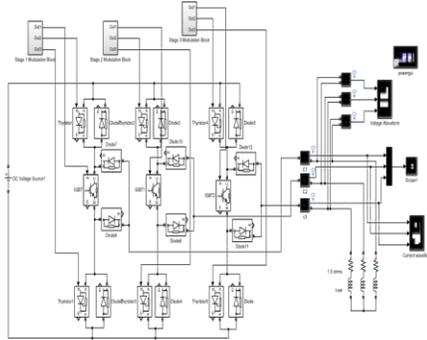


**Fig 7:.**MATLAB/Simulink Model of VSI

THD without Filter is 45.13%
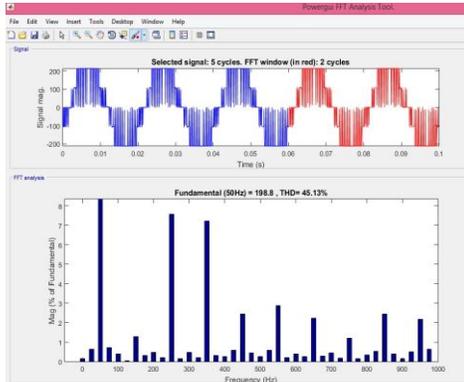


**Fig 8(a):** THD of Voltage Waveform without Filter
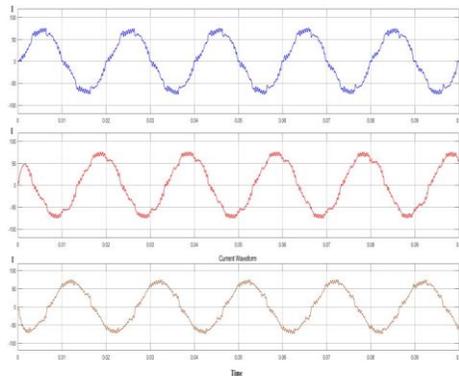


**Fig 8(b):** Output Current Waveform without Filter

THD of current with RL load is 10.6% without filter.
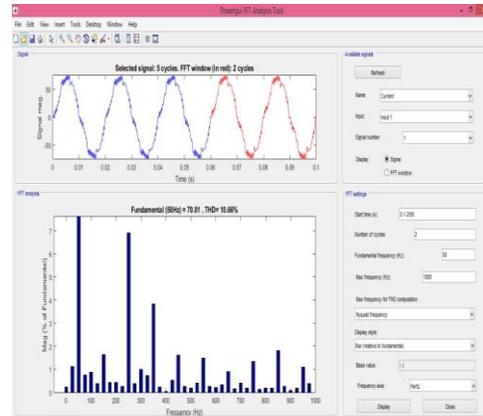


**Fig 8(c):** Current THD with RL load without filter

After using filter, we get the results given below
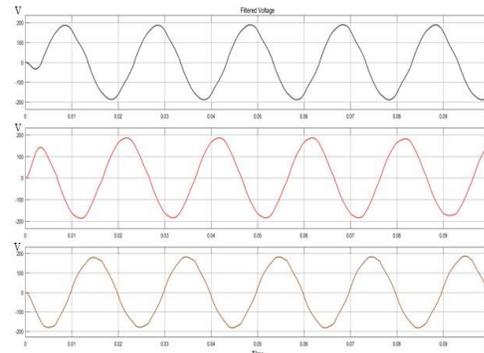


**Fig 9(a):** Voltage Waveform after Filtration

THD of Voltage waveform after filtration that is 3.03%
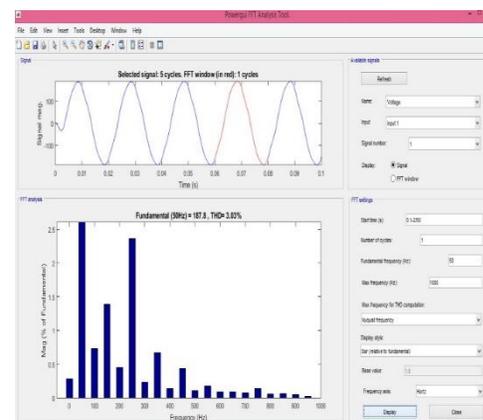


**Fig 9(b):** Voltage THD after Filtration
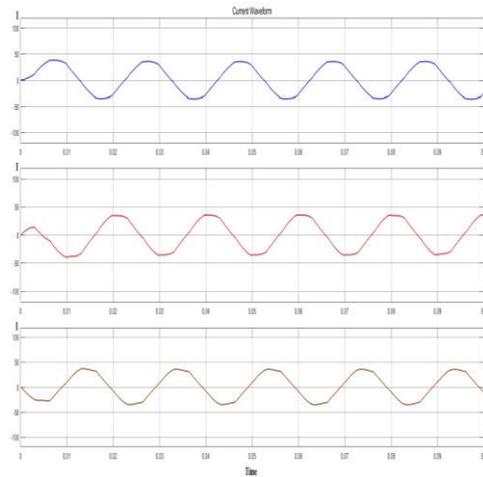
**Fig 9(c):** Current waveform after Filtration

Current THD after filtration is 2.89%
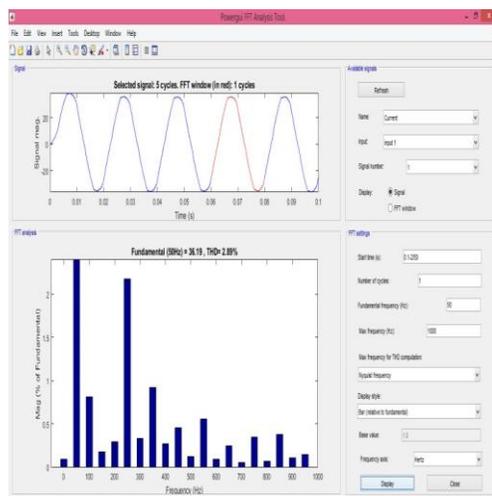


**Fig 9(d):** Current THD after Filtration.

Finally, Figure 8(a) shows the output three-phase line voltages and Figure 8(b) shows the output three-phase current waveform without filter. All the outputs are taken as a PWM technique which can be further improved by using different technique. Also, results are shown with filter in Figure 9(a) and Figure 9(b) three-phase line voltages and THD of filtered voltage respectively. Figure 9(c) and Figure 9(d) shows three-phase filtered current waveform and THD of current waveform.

## 7.     Hardware Results

This Novel topology of Voltage Source Inverter is also implemented on hardware to verify the results extracted from the simulation. Switches and components used to implement this topology are as following:

Input DC Voltage: 12-30 V (Peak to Peak)
Output Inductance: 10 mH;
Output Resistance: 1 KΩ;
Output Frequency: 50 Hz;
Arduino UNO: To give switching signal
BT151: Thyristor
IRG4BC40S: Transistor
PN-Junction: Diode



**Fig 10(a):** PCB Board with Components
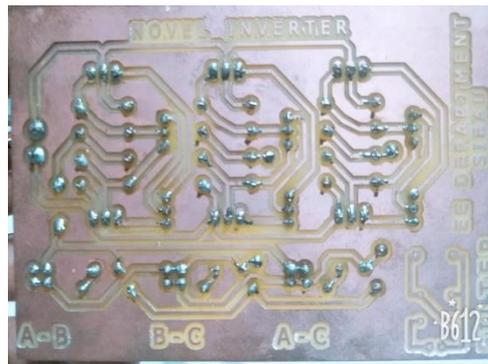


**Fig 10(b):** Circuit Design on PCB Board
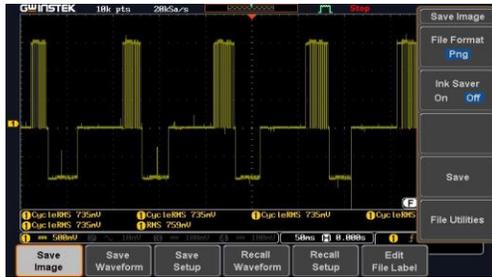
**Fig 10(c):** Experimental Result of output Waveform
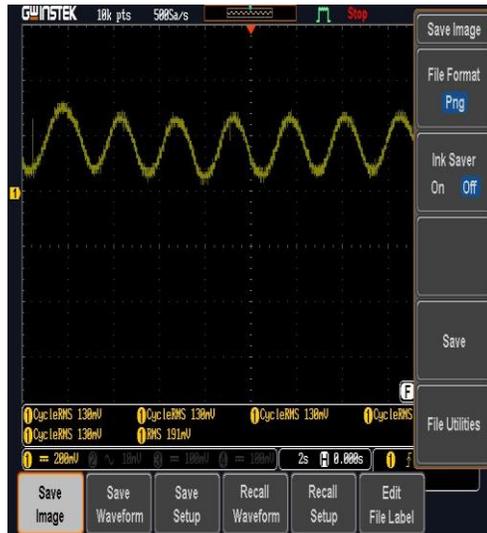


**Fig 10(d):** Output voltage wave of Novel topology after filtration
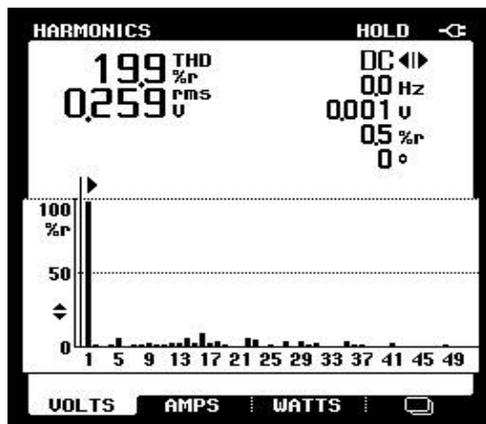


**Fig 10(e):** THD of filtered output Voltage

After getting output three-phase line voltages, it can be seen that this topology has the same features as the conventional topology in term of voltages. Although the waveforms are slightly distorted, it can be improved by developing and utilizing better switching technique and control scheme. In addition, current wave form will be given soon by implementing new scheme. In future, some steps would be taken to make this topology in use for the domestic as well as commercial use.

## 8. CONCLUSION

Voltage source (VSI) and current source inverters (CSI) are widely utilized in various applications such as, adjustable speed drives (ASD) for AC motors, induction heating, uninterruptable power supplies (UPS), standby power supplies, electronic frequency changer circuits, distributed generation units, HVDC systems to name a few [11],[12]. From the above results of MATLAB/SIMULATION as well as of hardware results, it can be seen that the novel topology of voltage source inverter has the same features in terms of voltage-current waveforms provided in both sections i-e Simulation and Hardware. Although, some results are distorted, these distortions can be mitigated by using more appropriate switching schemes, controlling schemes and more authentic filtration methods. Observed from above results, the Novel topology has advantages of THD over the conventional inverter as well as it has an advantage of its application that it can be used for high power applications. Furthermore, this topology can be expanded to the domestic purpose as conventional topology is tending for domestic purpose. As the novel topology can be an economical alternative for the domestic purpose, it has a benefit of low cost as compared to the conventional topology. By taking some serious initiatives, this topology can be introduced to the domestic market for the betterment of society. The main purpose of this paper was to realize the importance and advantages of novel topology of voltage source inverter over the conventional topology.

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