Vol. 1, No. 2 | July - December 2018

A Novel Asymmetric Three Phase Multilevel Inverter with Reduced Switches

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Abstract:

Multilevel inverters (MLI) are the most reliable and suitable inverters for medium and high-power applications. These inverters reduce the total harmonic distortion. There exist many types of single and three-phase multilevel inverters which are used in industries. The main issue of these multilevel inverters is use of an excess number of switches, which introduces the in-system losses, complexity of circuit, size, and cost etc. There are many novel topologies of multilevel inverter which are addressing the same issues. This paper anticipated a new topology of asymmetric cascaded multilevel inverter (MLI). This novel topology can be used for single, three and multi-phase inverters and is most suitable for medium and high-power applications. To demonstrate the working of this novel topology in detail, its modes of operation are also explained. The validity of this inverter is tested for both resistive and inductive load. Due to the utilization of very limited switches, gate drivers and DC voltage sources, it is found that this topology is low cost, simple and efficient inverter.

Keywords: *Three phase multilevel inverter, Cascaded Multilevel Inverter, medium power, and high-power converters, Asymmetric Multilevel Inverter, Reduce switches*.

1. Introduction

Multilevel inverters (MLI) synthesize several DC voltage sources to produce staircase output having desired multilevel waveform [1-3]. Multi-level inverters are the modification of basic bridge inverters. They are normally connected in series to form stacks of level. Multilevel inverters (MLI) are widely used in medium power and high-power applications [4-6]. There is a lot of interest in multilevel inverters due to its usage in renewable energy resources [7]. Total harmonic distortions (THD) in MLI are low. That is why they are also preferable for industrial motor drives [8]. MLI are also used in flexible transmission system, where it is a core component of STATCOMs.

Multilevel inverters (MLI) exist as single, three and multi phases in industry. In this paper, we targeted three phase inverters. Three classical topologies of MLI are: (a) neutral point clamped MLI (NPC) [9], (b) cascaded H-bridge MLI (CHB) [10, 11], and (c) flying capacitors MLI (FC) [12]. Type (a), Cascaded H-bridge is the most favorable among these three classical topologies for applications requiring many levels. Type (b) neutral point clamped Inverter (NPC) are used in applications requiring lesser number of output levels. Type (c) Flying capacitors topology has the advantage of modular structure, minimum

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requirement of DC voltage sources and low-cost components. Due to large interest in cheaper, reliable, and better quality multilevel inverters a lot of research is ongoing to design optimum multilevel inverters. Research areas like reducing numbers of switches and others power components in converters design is one of the most interested area for researchers [1, 8, 13, 14], while number output voltage levels of the inverter are not disturbed.

By growing the number of output levels in inverter, the harmonic distortion reduces, and hence output waveform quality improves. With increase of output levels, the number of switches also increases dramatically. The increase number of switches reduces efficiency, while increases size, complexity, and cost of the system. In this research, a novel asymmetric MLI topology is anticipated to achieve desired output levels with fewer number of switches and gate drivers. A work like this research is listed in [10, 15, 16]. The proposed design is based on a modified version of cascaded topology; therefore, hereafter discussions is restricting to the cascaded topologies only.

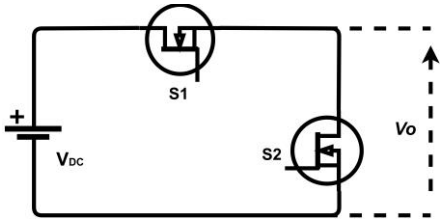

Fig. 1. The unit cell of MLI

The number of bridges required in the CHB inverter is proportional to the number of output staircase levels. The mathematical relationship between number of levels (NL) and number of bridges (NB) required is given as:

$$N_B = \frac{N_L - 1}{2} \qquad (1)$$

NL can be any odd integer greater than three. Similarly, the total number of switches required NT are:

$$N_T = 4N_B \qquad (2)$$

By combining equations 1 and 2 number of required transistors can also be represented as:

$$N_T = 2(N_L - 1) \qquad (3)$$

The topological structure of MLI must have the capability to deal with the following points

- Capability to sustain high input voltage such as HVDC
- MLI must have less switching devices as possible.
- Low switching frequency for MOSFET's/IGBT's due to multilevel approach.

Similar work is presented in [15] which also addressed the importance of reduction of switches and anticipated a novel MLI with reduced number of switches. As proposed in [15] it is concluded that for addition of a new source to increase a positive and a negative level two transistor switches are required in the case of symmetric MLI. For the ease of access, the unit cell used in [15] to increase 2 levels of the output is depicted in figure 1. It is clear from the figure 1 that S1 and S2 are the required two switches while the Vdc is the voltage to be synthesis with the output.

A similar work is also presented in [16] where the proposed inverter also synthesis two levels with a single switch with the output but the transistor used in that topology is a bidirectional switch, where two transistors are connected back to back. While comparing the inverter proposed in this research is using only unidirectional switch along with only an additional switch.

In the similar way the unit cell used in this research (Asymmetric cascaded MLI) is consist of a voltage source, a transistor and a diode as shown in Figure 2. Hence one transistor in the inverter of [15] is replaced with a diode. The replacement of transistor with diode is giving good results in many aspects. The most prominent advantages are no turn ON and OFF of diode are required. Therefore, it decreases the complexity of

control signals. The diode is more robust than transistors. High power rating diodes are usually more easily available than transistors, it also decreases the cost of inverters because usually diodes are cheaper than transistors. Furthermore, the diodes do not need any driver circuitry, therefore, it further reduces the cost, size, and complexity of the circuit.

This proposed design is further explained in detail in the section II of this paper.

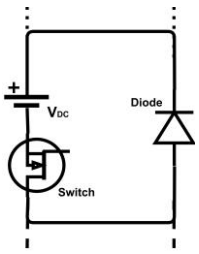

Fig. 2. Unit cell of the proposed Asymmetric cascaded MLI

Table I shows comparison between classical cascaded topology, Diode clamped MLI topology and proposed novel MLI topology. The number of switches is quite less than those of the two other topologies as shown in table I. Number of levels increases with the number of switches increases drastically. On the other hand, novel MLI topology requires only one switch to introduce new level.

According to the above discussion and calculation the following table shows the relation between the classical cascaded H-Bridge inverter, the reduced switches inverter discussed in [15] and proposed multilevel inverter topology.

This research is organized such as, section 2 explains the proposed design. Section 3 explains the modes of operation, while in section 4 the design is validated using simulations. In section 5 the modulation technique has been discussed. In section 6 the design is tested for inductive load. In section 7 hardware implementation has been discussed section 8 the conclusion has been made and at last future work has been proposed.

2. PROPOSED MULTILEVEL INVERTER TOPOLOGY

This research proposed a new topology of asymmetric cascade MLI in which two levels (one positive and one negative) are added to output by the addition of a single transistor and diode as shown in Figure 3. Although this topology is general and can be extended to any levels here just for simplification we limited our discussions to 5 levels. For five levels output our topology requires an H- bridge (consisting of four transistors), one diodes and one transistors (along with anti-parallel diode) switches as compared to classical inverter that requires 8 transistors, this new design significantly reduces the number of required switches and the number of gate drivers along with another required circuitry. Comparison has been shown in table II.

TABLE I. Comparison of Topologies with reduced switches

No. of levels	Classical Cascaded H-Bridge Topology A		Diode Clamped Topology B		Proposed Reduced switches Cascaded Topology B	
	Number of transistors	Number of drivers	Number of transistors	Number of drivers	Number of transistors	Number of drivers
5	8	8	8	8	5	5
7	12	12	12	12	6	6
11	20	20	20	20	8	8
13	24	24	24	24	9	9
N	2n-2	2n-2	n+3	n+3	(n-3)/2+4	(n-3)/2+4

TABLE II. Comparison of Topologies with reduced switches

	Diode Clamped MLI	Flying capacitor MLI	Cascaded MLI	MLI with Reduced Switches
No. of Switches	8	8	8	5
No. of Clamping diodes	8	0	0	1
No. of Floating capacitors	0	8	0	0
No. of dc bus capacitors	4	4	2	2

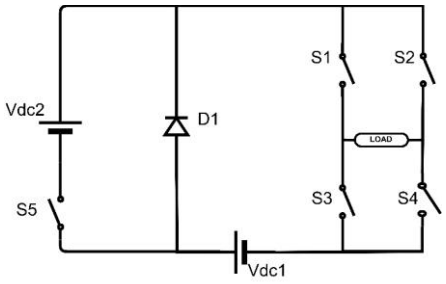

Fig. 3. Asymmetric cascaded MLI

The number of transistors switches (NT) for any desire levels can be found as:

$$N_T = \frac{N_L - 3}{2} + N_B \qquad (4)$$

Where NL is the number of desired staircase output levels and NB is denote as the number of transistors in H-bridge.

To generate multi-level output the design requires isolated DC voltage sources and diodes. These isolated DC sources to synthesis and number of extra diodes is a function of output levels which can be formulated as:

$$V_{DC} = \frac{N_L - 3}{2} + 1 \qquad (5)$$

$$N_{DL} = \frac{N_L - 3}{2} \qquad (6)$$

$$N_{FD} = N_T \qquad (7)$$

Where, VDC stands for isolated DC voltage sources and NDL represents number of diodes requires for addition of levels to the output. In addition, freewheeling diodes (NFD) require are also given by equation 4.

2.1. Case Study: Nine Level Inverter

In this section, a single phase of the proposed design is explained by considering the case of nine levels output. By using equations 4, 5, 6 and 7 we found number of transistors, freewheeling diodes. Figure 3 shows the circuit diagram of the five levels MLI.

The design is validated by using simulations presented in Section IV which is

TABLE III. Switching Scheme

S1	S2	S3	S4	S5	Output Voltage
ON	OFF	OFF	ON	OFF	Vdc1
ON	OFF	OFF	ON	ON	Vdc1 +Vdc2
OFF	OFF	OFF	OFF	OFF	0
OFF	ON	ON	OFF	OFF	-(Vdc1)
OFF	ON	ON	OFF	ON	-(Vdc1 +Vdc2)

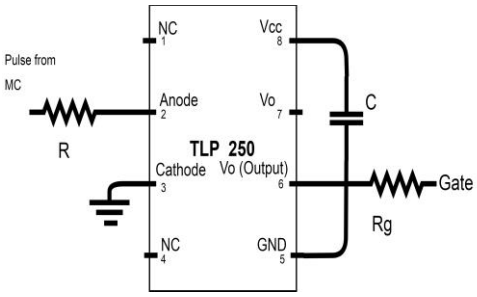

Fig. 4. Driver Circuitry

also tested for inductive load presented in section VI. The working principle of the design is explained in next section.

2.2. Gate Circuitry

TLP 250, like other drivers has an input stage, output stage and the input power source. It is optically isolated driver, means that input and output are optically isolated. Figure 4 shows the diver circuitry.

3. WORKING PRINCIPLE

Table III shows the switching scheme of the Novel single phase five level asymmetric cascade MLI topology, given in figure 3. The working of the design is explained by using five modes, where positive half cycle is explained by using modes 0 to 2. Negative cycle is explained by using modes 3 to 4.

3.1. Positive Half Cycle

The positive half cycle is given in figure 5. To achieve the waveform of figure 5, the entire procedure and switching scheme is divided into three different modes, which are discussed below in detail with heading Mode 0 to Mode 2.

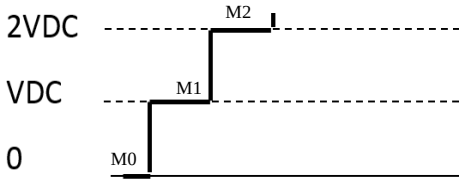

Fig. 5. Positive half cycle

Mode 0: In this mode no switch is conducting, so the output voltage is V=0 which is shown in Figure 6 and its output is highlight with M0 in Figure 5.

Mode 1: In this mode Switch 1 and Switch 4 are in ON state, along with diodes 1 that is in forward conducting mode. The voltage source VDC1 is connected to load as shown in Figure 7 and figure 5 shows first stair in output appears as M1.

Mode 2: In this mode of operation, diode D1 is turned off while switch 5 has been turned ON in addition to previous switches. In this mode two voltage sources VDC1 and VDC2 add up and are connected to the load as shown in Figure 8 and output stair is highlighted with M2 in Figure 5.

Mode 2 completes the positive half cycle; the next positive half cycle is generated by reversing the aforementioned modes in which the output level decreases gradually and at last reach to zero level in which no source is

connected to the load using transistors. In this case, if the load is inductive, the stored energy can be sent back to the sources using freewheeling diodes.

3.2. Negative Half Cycle

Similarly, to the positive half cycle the level of the inverter increases in negative region by adding the DC voltage sources with load in reverse polarity. The output levels are shown in Figure 12. The whole process and switching scheme utilized in generating of negative half cycle is explained in detail in Mode 3 and Mode 4.

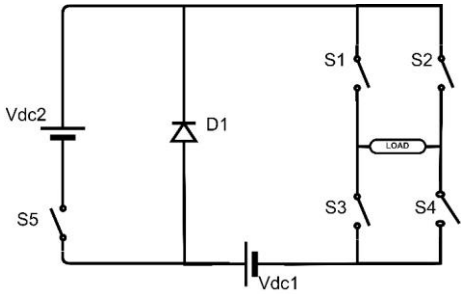

Fig. 6. Mode 0

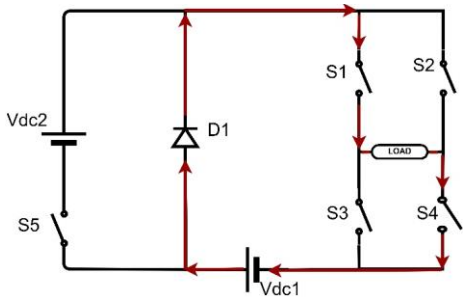

Fig. 7. Mode 1

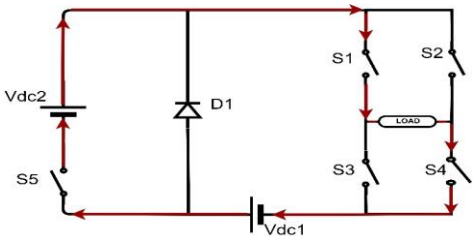

Fig. 8. Mode 2

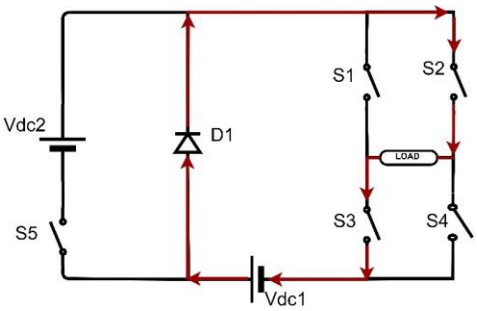

Fig. 9. Mode 3

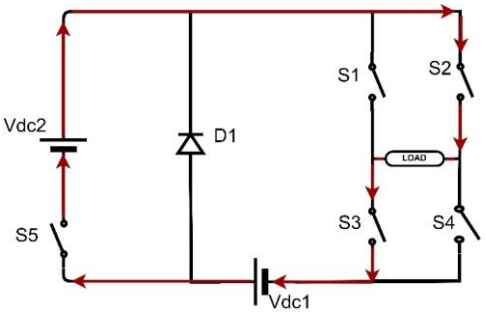

Fig. 10. Mode 4

Mode 3: In this mode Switch 2 and Switch 3 are turned ON, while the diode 1 is in forward conducting state as shown in Figure 9 with this switching scheme the voltage source VDC1 appears across the load with negative polarity that is Vout = -V as shown in Fig 12, which is highlighted as M3.

Mode 4: In this mode, switch 5 is conducting, while the diode D1 is turned OFF and the remaining switches are in same state of conduction as that of Mode 4. So, the sum of DC voltage sources VDC1 and VDC2 connect to the load with negative polarity as shown in figure 10 and figure 12 shows the output as M5.

Mode 4 completes the negative half cycle of the staircase output; the next negative cycle is generated by reversing the modes in which the output level decreases gradually from negative peak value and at last reach to zero level in which no DC voltage source is connected to the load using transistors.

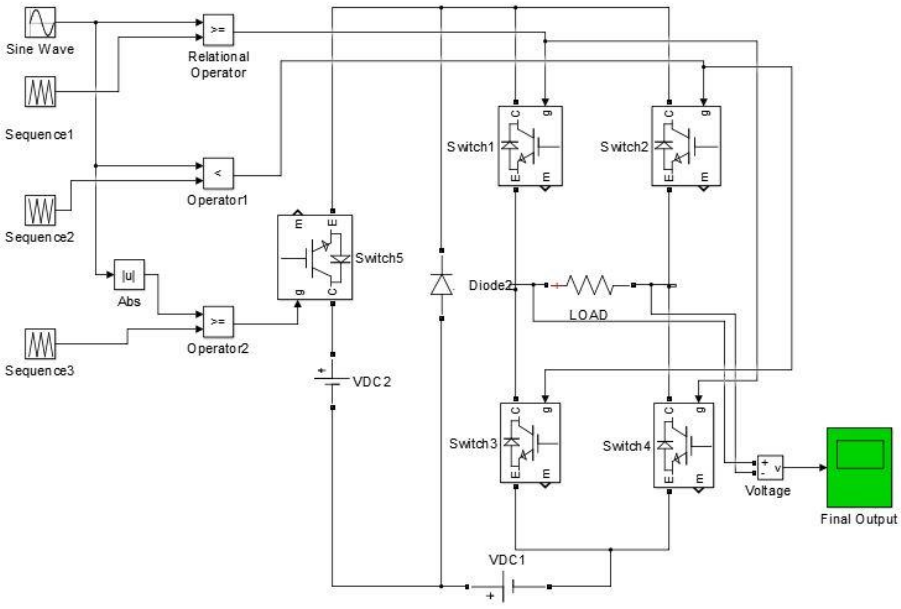

Fig. 11. Single phase of Five level multilevel inverter

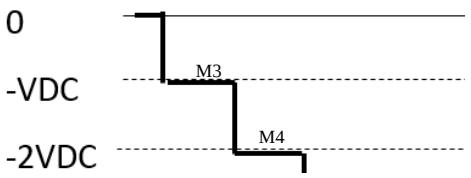

Fig. 12. Negative half cycle of output

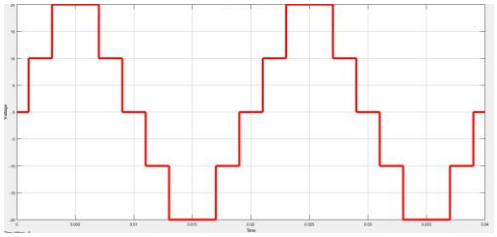

Fig. 13. Simulation results five level single Phase Multilevel Inverter

All the above 5 modes discussed for 5-level multilevel inverter. Simulation results for 5-level MLI has been discussed in the coming sections.

4. SIMULATION

The novel MLI design has been validated by using MATLAB/Simulink toolbox. Simulation has been performed for the design given in Figure 3 for generating five levels output. Figure 11 shows the simulation model of proposed novel single phase MLI. In the simulation for five level MLI, five switches and one diode are used. The staircase waveform for resistive load is shown in the fig 13. This makes the output wave form to look like sine wave, the width of the output stairs is different.

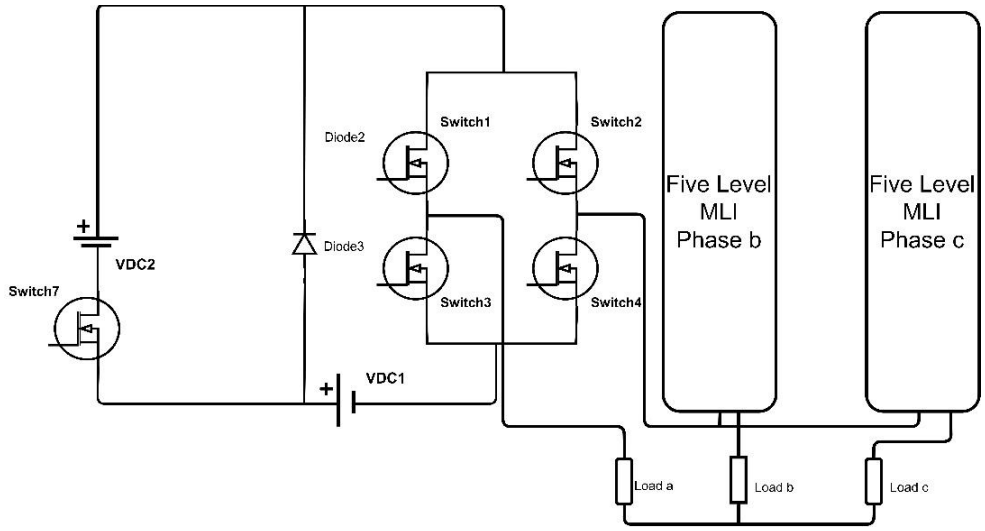

Fig. 14. Three Phase Asymmetric cascaded MLI

In the similar way, proposed design of five-level three phase multilevel inverter has also been implemented using MATLAB Simulink. The three-single phase MLI of Figure 14 are connected in parallel to generate 3-phases as shown in Figure 16.

The simulation results are shown in Figure 16 is the out from phase to neutral.

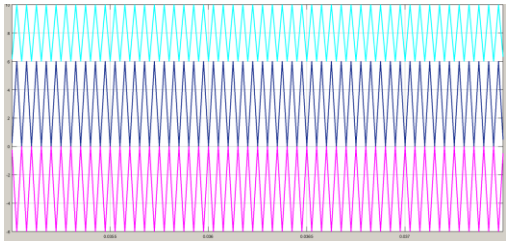

Fig. 15. Carriers Signals for MLI

5. SINEWAVE PULSE WIDTH MODULATION (SPWM)

To regulate the output and control different parameters of inverters modulation techniques are used [20]. There are many types of modulation techniques for the modulation of the proposed MLI [21-22]. Here to verify the validity of modulation in the proposed MLI, shifted carrier based SPWM is selected and used. Alternate Phase opposite Disposition

(APOD) has been used for modulation as shown in figure 15. In APOD modulation all carriers are in phase that are above the zero-reference level but are opposite to triangular signals below zero reference. Normally four triangular signals will be required, but for this topology, three triangular signals are sufficient. Switch 5 is ON in both intervals (+ive and -ive), So, it required one triangular signal.

The test is conducted by using carrier frequency 20 kHz while the modulated frequency is 50 Hz and for nine level MLI.

Here the carriers are the triangular waves while the modulated signal is a reference sine wave. The carriers are compared with the reference sine wave and the desired switching pattern of transistor gate signal is generating. The modulated output wave form for single phase is given in Figure 17 and for three phase outputs is shown in figure 16. Figure 18 shows the harmonic analysis of MLI. The total harmonic distortion is 5.82%.

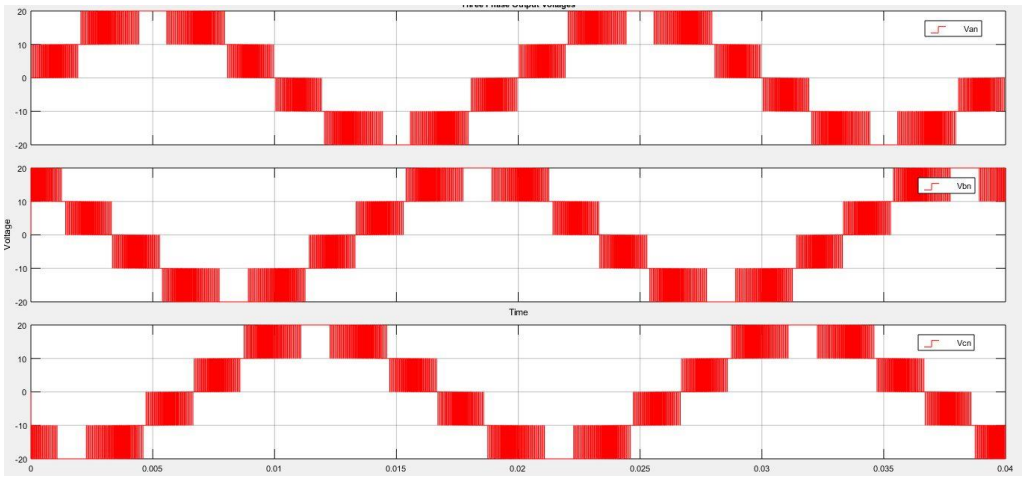

Fig. 16. Three Phase MLI SPWM Modulated Output

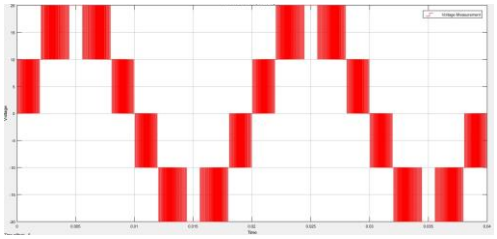

Fig. 17. SPWM modulated output waveform

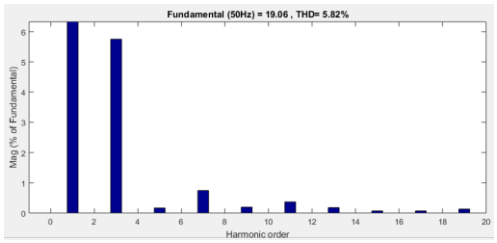

Fig. 18. Hamonic Analysis

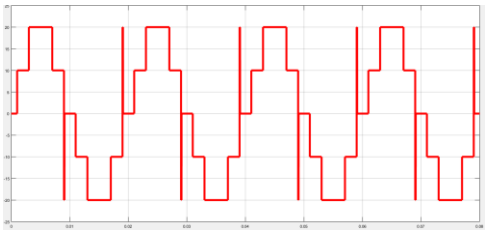

Fig. 19. Output wave with inductive load

6. VALIDITY FOR INDUCTIVE LOAD

The validity of the proposed MLI is also tested for inductive loads. Fig 19 shows the simulation model with inductive load. There are anti-parallel diodes with each transistor which is working as the freewheeling diode when the reverse e.m.f. produces during switching in the presence of inductive load.

7. HARDWARE IMPLEMENTATION

A prototype has been developed for the proof of concept of proposed MLI. This prototype of inverter is given in Figure 20. The triangular and reference sine wave are generated by using op-amp ICs while for the comparison of the two signals comparator ICs are used. Probe has been set with 10x and vertical sensitivity is 1 volt/cm.

$$V_{p-p} = 50\ V$$

$$V_p = \frac{50}{2} V$$

$$V_p = 25\ V$$

Figure 20 shows the three-phase implementation of five level multilevel inverter. Second shelf has the push pull inverter for low voltages (24 low voltage supplies). Third shelf has the circuit for

switching signals. The output wave of the prototype is given in the Figure 21. Due to unavailability of three channel oscilloscope only single-phase output is given in Figure 21.

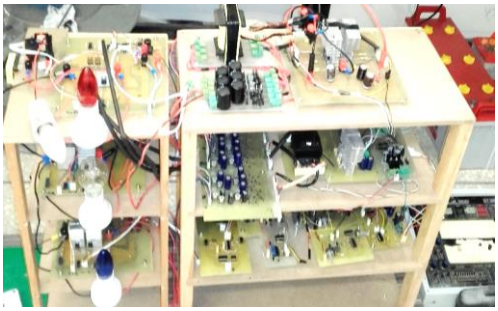

Fig. 20. Three phase multilevel inverter prototype

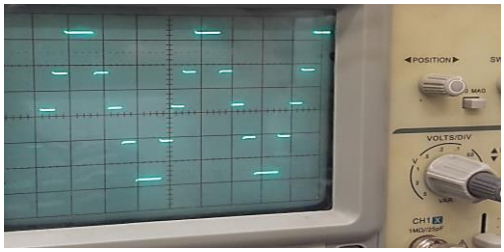

Fig. 21. Single phase output of MLI prototype

8. CONCLUSION

The Novel topology of an asymmetric cascaded MLI has been proposed that has less number of switches. The design reduces switch losses and is more cost effective. Therefore, the number of driver circuit is also reduced, as well as low dv/dt stress on individual switch and switching losses is reduced. As the number of power components decreases, the cost decreases, the design becomes simpler and size of the system also reduces. The design can be used to generate output waveform with any desired number of levels. The proposed design has been validated by simulations considering resistive as well as inductive loads.

9. FUTURE WORK

More modulation techniques like SHEPWM, SHMPWM, etc. can be applied to this novel topology to further reduce total harmonics distortion THD.

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