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FPGA-Based Implementation of Algortham Architecture Co-Optimized Adaptive Noise Canceler Using Sigma Delta Modulation

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Abstract:

As FPGA has been in trend for a few decades in prototyping simple to complex Digital Signal Processing (DSP) systems, some issues are still highlighted in FPGA-based implementations. One issue is the limited resources available onboard. Optimization has always remained a choice of developers, either hardware or software-based. Algorithm architecture co-optimization is a domain that incorporates some changes in existing algorithms besides bringing some ways to produce compact architecture. One of the methods in architecture optimization is to apply short-word length-based DSP systems that use a sigma-delta modulation (SDM) approach to reduce the actual data word length from multi-bit to single-bit. SDM in the design causes the system to become compact and efficient. This paper produces algorithm architecture co-optimization for the application of adaptive noise canceler for wireless communication. The algorithm taken is SDM-based Steepest-Descent, and its implementation is compared with the new proposed SDM-based correlation-less design. Both approaches are simulated in MATLAB, and their functional verification is carried out along with comparing some statistical parameters, including SNR, MSE, and PE. Besides, both the designs are translated on Vertex-7 FPGA to verify the less resources consumed by the proposed method. The MATLAB and FPGA-based results indicate that the proposed design may be the best choice for less sensitive applications, like voice or video while the proposed design is a generic solution that may apply to any noise value.

Keywords: *Sigma-Delta Modulation; Adaptive Filter; MATLAB; FPGA; Optimization*

1. Introduction

The resources limited ASIC or FPGA gets saturated when complex DSP algorithms are directly translated on them[1, 2]. Optimization at the algorithm or architecture level is adopted as a solution. Sometimes, the algorithm and architecture co-optimization makes the design even more compact [3]. One of the latest methods of resource reduction in ASIC or FPGA-based implementation is sigma-delta modulation, which was initially introduced for analog to digital conversion but is now used for word length reduction [4].

Various SDM-based DSP applications for word length reduction and hence reducing the overall system complexity are reflected in the literature that includes but is not limited to simple arithmetic units [5-7], FIR filters (fully

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or partially transformed to single-bit) [8-15], IIR filters [16-18], and some complex adaptive filter structures [19-22]. Other recent examples of SDM-based short word length systems include adaptive channel equalizers using a µ-less approach [23], Weiner filters [24], Matched filters [25], digital arithmetic units [26], smart sensor communications [27], correlation-less filters [28, 29] and latest SDM-Based Image Processing [30].

As mentioned above, algorithm-level optimization produces a more compact design in hardware-based implementation (like ASIC or FPGA) besides optimizing the architecture [31]. This concept is validated in work in [32], where the authors have proposed and implemented an autocorrelation-less Wiener filter and have compared it with a conventional Wiener filter design. The results show that the proposed correlation-less approach may be an excellent variant of its conventional method.

In continuation of that work, in this paper, the authors propose the SDM-based autocorrelation-less Steepest-descent algorithm for the application of adaptive noise canceler and compare it with conventional SDM-based design.

In wireless communication, the channel noise variance has an impact on SNR, and accordingly, SNR has an impact on MSE and PE, so in parallel to functional verification, these statistical parameters are also taken into consideration and simulated using MATLAB.

Then the design is implemented in vertex - 7 FPGA to see the impact of algorithm architecture co-optimization.

The results indicate that the proposed SDM-based autocorrelation-less Steepest–descent filter gives the same filter output as that filtered with an SDM-based conventional filter. Also, implementing the proposed model on FPGA results in less resource consumption compared to a simple SDM-based approach.

Hence, the SDM alone results in the area-optimized implementation of complex DSP systems. However, when the algorithm optimization is carried out along with SDM, a dramatic reduction in resources and an increase in achieved operating frequency are observed.

These results make the autocorrelation-less SDM-based approach more suitable for less sensitive applications requiring less resource consumption, like voice or video communication, while the scope of the work is generic and may be applied for any noise value, evident in the noisy channel.

The paper further proceeds as follows: Section 2 of the article proposes the architecture of SDM-based correlation less filters, which is simulated in MATLAB, and the results are shown in section 3. For hardware-based validation of the proposed design FPGA FPGA-based implementation is also carried out, and the result is reported in section 4. Finally, in section 5, the conclusion of the work is reported along with the future intentions of the work.

2. Proposed Architecture of Steepest Descent Approach Based Adaptive Noise Canceller.

The Steepest-descent algorithm has many applications in DSP, especially in adaptive filters. When the data is transmitted through a communication channel, it undergoes distortions due to channel perturbations. To get rid of it is to design an inverse filter that behaves reciprocal to the channel and mitigates its impact. The design of inverse filters is mainly carried out with adaptive filters-*adaptive reflects the concept of adaptation that means with a change in environment, the filter tabs would get changed*.

In some cases, the data can be victimized by the noise, along with channel degradations. An extra factor is added to the inverse filter for noise removal to provide dual functionality. The concept is elaborated in Fig. 1.

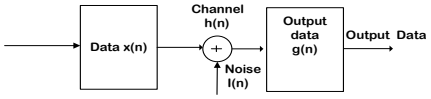

Fig. 1: Addition of Noise into Data through Transmission Channel.

In Fig. 1, f(n) is the input data we need to transmit through the channel, with the impulse response h(n). Some random noise I(n) may be added to the signal via transmission. So the received data, g(n) becomes:

$$g = f(n) * h + I(n) \qquad (1)$$

In equation (1), f (n) is convolved with h(n) in the time domain. Sometimes convolution becomes complex to deal with. It is better to convert it into the frequency domain, which is translated to multiplication. The frequency domain representation of equation (1) is given in equation (2).

$$G(N) = F(N).H(N) + I(N) \qquad (2)$$

At the receiving end, we have the degraded signal G(N). However, we are interested in finding original data F(N) from that degraded data, so by rearranging equation (2), we can get our desired term in equation (3).

$$F(N) = \frac{G(N)}{H(N)} - \frac{I(N)}{H(N)} \qquad (3)$$

In equation (3), the first term $\frac{G(N)}{H(N)}$ is the ratio between the received data to channel impulse response and is generally known as an inverse filter. Another term is the ratio of noise to channel impulse response, and we are more interested in finding the noise term as the channel behavior may be obtained by the experiments.

To adjust this noise term, we need to use a Steepest–descent-based filter that is better than the inverse filter as it incorporates both the degradation function (H(N)) and the statistical parameter of the noise (I(N)).

The Steepest-descent-based filter is the class of adaptive filter that gets its weight updates based on the error value.

The algorithm works on three signals, input, filtered, and desired. The input signal has a noise component in it; the filtered signal is achieved as an output, while the desired signal (replica of the input data that is sent before the receiver introduces some delay into it to adjust the delay that the channel may produce) is a noise-free signal that we wish to achieve. The comparison of the desired signal and filtered signal results in an error that intern helps in the filter's weight adjustments and as a result the filtered signal gets very close to the desired signal.

If F^ (N) is the desired data and G(N) is the received data, then the error between the two data may be calculated as $E^2 = E(G - F^{\wedge})^2$. The theme of the Steepest-descent algorithm is to minimize this mean square error (objective function) and to get the output data as the replica of the desired data. The block diagram of the conventional adaptive noise canceller is given in Fig. 2.

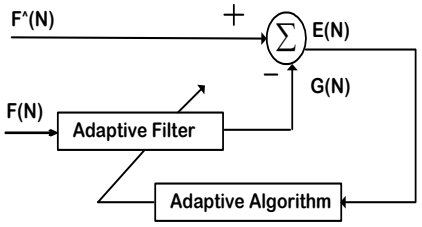

Fig. 2: The Block Diagram of Covnevtional Adaptive Noise Canceller.

The conventional approach of SDm-based steepest-descent-based adaptive noise canceller is shown in Fig. 3, and the proposed SDM-based correlation-less design is in Fig. 4. In both the architectures, the total number of input samples and desired data is set to 60000. The input and the desired data (delayed replica of information) are passed to the adaptive filter that calculates the autocorrelation matrix and cross-correlation vector between the two data sets and gets the filter weights updated accordingly.

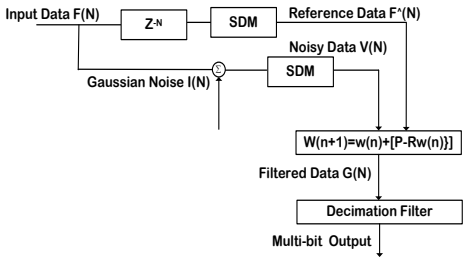

Fig. 3: Detailed Diagram of Conventional SDM- Based Steepest-Descent Algorithm for Noise Removal.

The proposed filter passes the reference and desired data through the SDM block containing OSR. After passing through the OSR block with OSR 8, each sample's total number of bits would be eight times higher than the original data rate. These single bits are then sent to the Steepest-Descent -based filter for calculating autocorrelation matrix R and cross-correlation vector P.

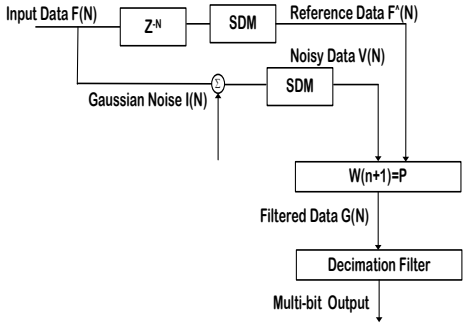

Fig. 4: Detailed Diagram of Proposed SDM-Based Corellationless Steepest-Descent Algorithm for Noise Removal.

3. MATLAB-Based Simulation and Results

The conventional and proposed architecture of the Steepest-Descent-based adaptive noise canceller is simulated in MATLAB, and the results produced are reported in various proceeding paragraphs.

An input sound wave is mixed with a randomly generated noise having a variance of 0.03. The noise is reflected in Figure.5

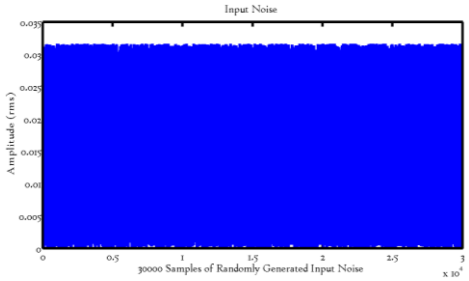

Fig. 5: 3000 samples of Randomly Generated Noise.

While simulation, 60000 input samples from the noisy sound wave were considered to be transmitted; Figure 6 shows 30000 samples out of those.

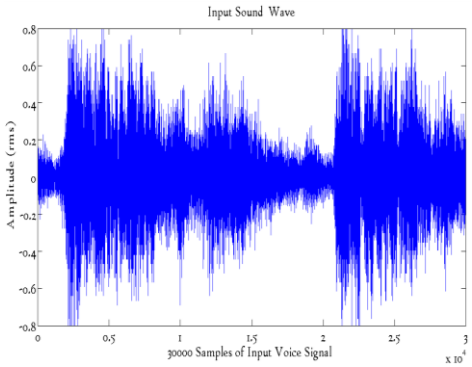

Fig. 6: 30000 Samples of the Input Sound Wave.

As the adaptive filter is based on the error estimation between the filtered and desired signals, producing the desired signal as the reference value at the receiver end is required. The desired signal is generated from the same input sound value with a delay of ten thousand samples. The delay would compensate for the real-time delay the signal may observe. Thirty-thousand samples of the desired signal and the filtered signal with the conventional Steepest-Descent algorithm are given in Fig. 7.

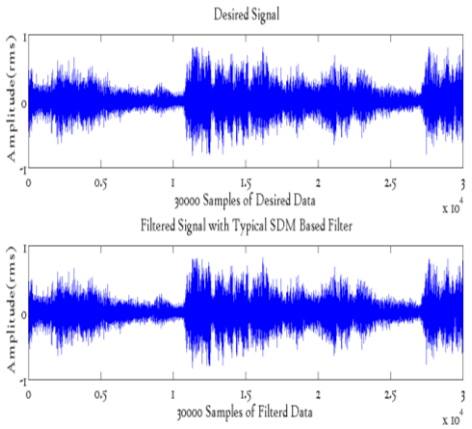

Fig. 7: 30000 Samples Desired Data and Filtered Data with Conventional SDM-based Approach.

While looking at the graph, it may easily be seen that the traditional approach perfectly

produces the replica of the desired signal, hence making the SDM an acceptable trend toward optimization.

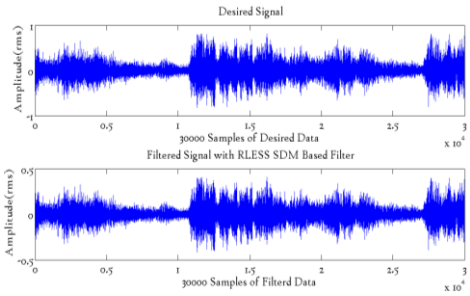

Fig. 8: 30000 Samples Desired Data and Filtered Data with R-Less SDM-based Approach.

As mentioned above, algorithm architecture optimization can still produce much better results. Hence, the graph below presents the justification for the statement and shows that the correlation-less approach provides a new way of achieving the same results even with reduced resources. One point to notice here is the filtered signal's amplitude, which is about half-db less than the desired signal. Most of the time, the receivers incorporate the repeaters or boosters to enhance the signal power, so this issue may need to be addressed or incorporated by adding some gain factor at the receiver end.

To see the difference between the outputs of the two filters, the error vector is calculated and plotted in Figure. 9 below. It may be observed that about 0.25 db of RMS values is generated as the difference vector.

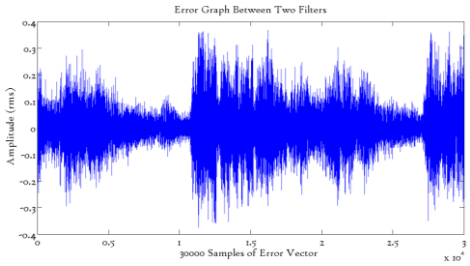

Fig. 9: 30000 Samples of Error Vector between Filtered Data with Conventional and R-Less SDM based Approach.

Some statistical characteristics are also considered to be analyzed to further look into the feasibility of the proposed system. The parameters taken are the variance versus signal-to-noise ratio, mean square error, and error probability.

The graph of Fig. 10 shows that with increased variance value, the SNR gets increased in both approaches. However, the conventional approach, the correlation-less method, has less SNR value, but even in the acceptable range of non-sensitive voice applications.

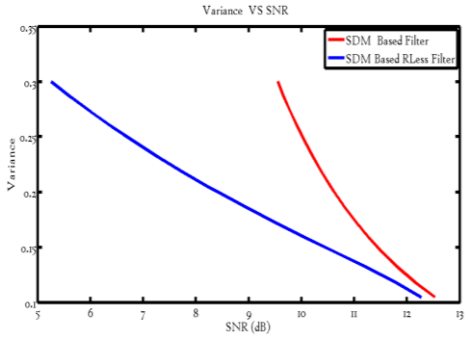

Fig. 10: Varianve VS SNR Relation in Conventional and R-Less SDM based Approach.

Similar to the SNR value, the mean square error increases with increasing variance value, which is the apparent phenomenon observed in communication. In contrast, the MSE of the proposed system is approaching conventional SDM-based design at less variance value and is 0.15 dB more at increased variance value.

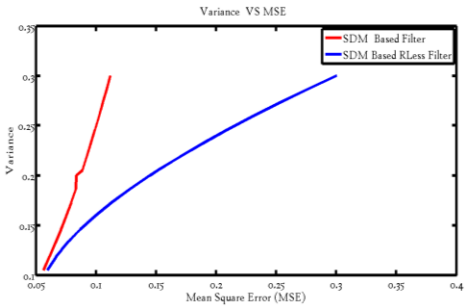

Fig. 11: Varianve VS SNR Relation in Conventional and R-Less SDM based Approach.

The last parameter compared is the variance versus probability of error. Like the other two outcomes, the PE value is proportional to the variance. While the proposed design exhibits more PE than the conventional approach.

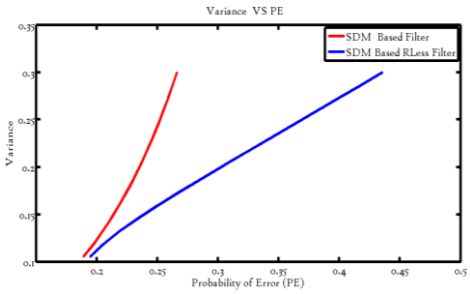

Fig. 12: Varianve VS SNR Relation in Conventional and R-Less SDM based Approach.

The functional verification and statistical analysis of the proposed design, produced in the above graphs, show that the SDM-based correlation-less approach may replace the conventional method at the cost of reduced amplitude and less SNR observed. While considering the voice as the targeted application, the proposed approach best suits the scenario where implementation resources are more concerned.

4. FPGA-Based Implementation and Results

The proposed SDM-based R_less approach and conventional designs are implemented in Xilinx verte-7 FPGA, with ISE 14.2 simulator.

For FPGA–based implementation, the input, and desired signals are produced in MATLAB, where each sample is represented as a floating-point decimal value. Before FPGA implementation, the floating-point decimal values are converted to IEEE-754, 32-bit floating-point data format supported by the FPGA synthesis tools. Only 50 input and desired data samples are derived for test purposes.

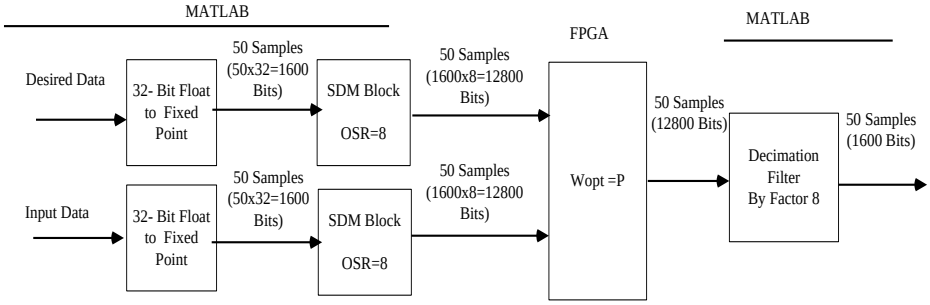

Fig. 13: MATLAB and FPGA Based Data Flow Diagram of Proposed Architecture.

Fifty 32-bit floating point data samples are presented to SDM –block where the oversampling ratio is set to 8. This means each 32-bit sample now would be converted into 256 single bits; similarly, 50 bits will result in 12800 bits. These 12800 bits of input and desired data will be moved to FPGA to perform data filtration. The filtered output contains 12800 bits that must be down-sampled by a decimation filter to reproduce the data rate.

The FPGA-based implementation of conventional SDM–based and proposed design is reported in Table 1. The consumed

resources include the lookup tables (logic elements of FPGA), multipliers, counters, and the performance parameter, including maximum achieved frequency and the path delay.

Table 1: FPGA-Based Implementation Results of Conventional and Proposed Design

FPGA Resource	Proposed Design	SDM Based Design
Number of Slice LUTs	15	37
Multipliers	4	9
Counters	1	3
Logic Level	2	4
Path Delay (ns)	2.917	3.917
Maximum Frequency (MHz)	342.806	255.29

It may be seen in the table that the conventional SDM-based design produces fewer resources, but when compared with the proposed approach, it has approximately twice more resource consumption with about 87 MHz less frequency. Hence it may be concluded that the conventional single-bit SDM-based correlation less Steepest-Descent approach provides algorithm architecture co-optimization therefore making it more suitable for applications requiring more resources.

5. Conclusions

In this research work, a method of optimization of a Steepest-Descent-based adaptive noise canceller is proposed, simulated, and implemented. In the proposed model, the weight update equation of the filter is kept correlation -less than in actual is not. The effect of this change has shown a negligible impact on the filter's performance, and also the simulations of statistical parameters indicate the acceptance of the proposed model.

Besides, the FPGA-based implementation of the proposed model shows a more compact and optimized design compared to the conventional one, along with the maximum operating frequency achieved.

These results open the door to accepting the Steepest-descent-based adaptive noise canceller in various applications that need adaptive signal processing.

In the future, real-time implementation of the proposed model will be carried out and compared with its counterpart.

AUTHOR CONTRIBUTION

All of the authors have contributed on a similar level in the implementation of the work and in preparing the paper draft.

DATA AVAILABILITY STATEMENT

The data will be made available upon request.

CONFLICT OF INTEREST

There is no conflict of interest between the authors or someone else. All the authors are listed in the correct order.

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